EEPROM cells divided into multiple non-overlapping sectors that individually contain a plurality of said cells sufficient to store multiple bytes of data and which are erasable together, comprising:

designating a first combination of a plurality of but less than all of said multiple sectors to be erased,

erasing the first combination of sectors without erasing others of said multiple sectors,

after the first combination of sectors has been erased, writing data in at least some of the erased first combination of sectors,

designating a second combination of a plurality of but less than all of said multiple sectors to be erased, wherein the second combination of sectors is different from the first combination of sectors,

erasing the second combination of sectors without erasing others of said multiple sectors, and

after the second combination of sectors has been erased, writing data in at least some of the erased second combination of sectors.

64. The method of claim 63, wherein erasing the first combination of sectors and erasing the second combination of sectors each includes:

verifying when individual sectors in the respective first or second combination of sectors become erased,

terminating further erasing of such verified sectors while continuing to erase others of the respective first or second combination of sectors, and

terminating further erasing of any of the respective first or second combination of sectors when all of the respective first or second combination of sectors have been verified as erased.

65. The method of claim 64, wherein designating the first and second combination of sectors each includes setting a tag bit for individual ones of the sectors to be erased, and wherein terminating further erasing of the verified sectors includes

clearing the tag bits for the sectors which have been verified.

66. The method of claim 63, wherein designating the first combination of sectors and designating the second combination of sectors each includes setting a tag bit for individual ones of the sectors to be erased, and wherein erasing the first combination of sectors and erasing the second combination of sectors each includes clearing the tag bits associated with the sectors that have been erased.

67. The method of claim 63, which additionally comprises maintaining an identification of those of said multiple sectors that are defective, and wherein erasing the first combination of sectors and erasing the second combination of sectors each includes avoiding the identified defective sectors.

68. The method of any one of claims 63-67, wherein erasing the first combination of sectors and erasing the second combination of sectors each includes erasing the respective combination of sectors in parallel.

69. The method of claim 68, wherein designating the first combination of sectors and designating the second combination of sectors each includes limiting the number of sectors that are erased in parallel in response to a predetermined power capability of the memory system.

70. A method of operating a memory system having an array of EEPROM cells divided into multiple non-overlapping sectors that individually contain a plurality of said cells sufficient to store multiple bytes of data and which are erasable together, comprising:

(a) initially tagging a plurality of said multiple sectors to be erased,

(b) subjecting the EEPROM cells of the tagged sectors in parallel to erase voltages while the remaining multiple sectors are not so subjected,

(c) thereafter verifying whether individual ones of the tagged sectors have become erased,

(d) clearing the tags from those sectors which are verified to have become erased while continuing to subject remaining tagged sectors to erase voltages, and

(e) repeating operations (b) through (d) until the tags have been cleared from all of the initially tagged sectors, thereby to erase all the initially tagged sectors.

2 1
71. The method of claim 70, which additionally comprises maintaining an identification of those of said multiple sectors that are defective, and avoiding subjecting such identified sectors to the erase voltages.

3 1
72. The method of claim 70, which additionally comprises limiting the number of sectors that are erased in parallel in response to a predetermined power capability of the memory system.

4 1-3
73. The method of any one of claims 70-72 wherein operation (a) includes initially tagging a plurality of but less than all of said multiple sectors to be erased.

5
74. A flash EEPROM system, comprising:

a memory controller and system address bus,

multiple sectors of flash EEPROM cells that are individually addressable through said address bus to be erased and which individually store multiple bytes of data, the cells of the individual sectors being erasable together when the individual sectors are addressed,

a logic circuit configured to address and enable for erasure, in response to signals from the controller, any combination of a plurality of but less than all of said multiple sectors, and

an erase circuit coupled to erase together all the enabled sectors without erasing others of the multiple sectors that are not so enabled.

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75. The system of claim 74, wherein the logic circuit includes a register associated with individual ones of the sectors to tag its respective sector as enabled for erasure.

1 6
76. The system of claim 75, which additionally comprises a verifying circuit that indicates when individual sectors have been erased, and wherein the logic circuit is responsive to said verifying circuit for clearing tags from those registers of a particular combination of sectors which are verified to be erased while maintaining the tags in the registers associated with others of said particular combination of sectors.

B1 4 5
77. The system of claim 74, which additionally comprises a verifying circuit that indicates when individual sectors have been erased, and wherein the logic circuit is responsive to said verifying circuit for disabling from further erase those of a particular combination of sectors which are verified to be erased while maintaining enabled for erase others of said particular combination of sectors.

9 5, 8
78. The system of any one of claims 74-77, wherein the erase circuit is coupled to erase all the enabled sectors in parallel.

10 5-8
79. The system of any one of claims 74-77, wherein the multiple sectors of EEPROM cells include substantially all the EEPROM cells in the system.

11
80. A flash EEPROM system, comprising:

multiple sectors of flash EEPROM cells that are individually addressable for erasure and which individually store multiple bytes of data, the cells of the individual sectors being erasable together,

a logic circuit configured to enable erasure of any one of multiple different combinations of a plurality of but less than all of said multiple sectors, and

an erase circuit coupled to erase together all the enabled

sectors of said any one combination without erasing others not in said any one combination.

12 11
~~81~~. The system of claim ~~80~~, wherein said logic circuit includes a plurality of registers that individually contain a tag indicating whether an associated sector is enabled for erasure or not.

13 12
~~82~~. The system of claim ~~81~~, which additionally comprises a verifying circuit that indicates when individual sectors have been erased, and wherein the logic circuit is responsive to said verifying circuit for clearing tags from those registers of a particular combination of sectors which are verified to be erased while maintaining the tags in the registers associated with others of said particular combination of sectors.

14 11
~~83~~. The system of claim ~~80~~, which additionally comprises a verifying circuit that indicates when individual sectors have been erased, and wherein the logic circuit is responsive to said verifying circuit for disabling from further erase those of a particular combination of sectors which are verified to be erased while maintaining enabled for erase others of said particular combination of sectors.

15 11-14
~~84~~. The system of any one of claims ~~80~~-~~83~~, wherein the erase circuit is coupled to erase all the enabled sectors in parallel.